Novel Electrical and Fluidic Microbumps for Silicon Interposer and 3-D ICs

Li Zheng, Yue Zhang, Gang Huang, and Muhannad S. Bakir

***Abstract*— Fine-pitch electrical microbumps (25-μm diameter and 50-μm pitch) and annular-shaped fluidic microbumps (150-μm inner diameter and 210-μm outer diameter) are presented to enable high-bandwidth die-to-die signaling, embedded microfluidic cooling and power delivery for silicon interposer and 3-D integrated electronic systems. Electrical and fluidic testing demonstrates good bonding of the electrical and fluidic microbumps; the average resistance of a single electrical microbump is 13.5 mΩ. The bonded fluidic microbumps are successfully tested up to 100 kPa without any leakage. Moreover, the power supply noise (PSN) of 3-D chip stacks is analyzed using a compact physical model. Based on the model, increasing the number of power/ground pads is effective in suppressing PSN, motivating the need for fine-pitch electrical microbumps. Impact of the number of dice in a stack, die thickness, and the area of on-die decoupling capacitors on PSN is also investigated.**

***Index Terms*— 3-D IC, flip-chip bonding, microbump, microfluidic cooling, micropin-fin heat sink, power supply noise (PSN), silicon interposer.**

I. Introduction

SILICON interposer (2.5-D) and 3-D integration technologies have attracted significant interest due to their potential in providing high-bandwidth low-energy die-to-die signaling, which is a bottleneck in modern high-performance computing systems [1], [2]. Moreover, they present other compelling advantages, such as a smaller form factor and heterogeneous integration [3], [4].

Compared with conventional organic and ceramic substrates, silicon interposers offer fine-pitch interconnects using conventional back-end of the line processes and fine-pitch microbumps for high bandwidth die-to-die signaling [5]. Moreover, silicon interposers eliminate the coefficient of thermal expansion mismatch between the silicon die and substrate [6]. Xilinx, Inc. has reported field-programmable gate array (FPGA) products using silicon interposers in which multiple FPGA dice are assembled on a silicon interposer with dense interconnects [7], [8]. Another example of recent interest in silicon interposer is the effort by IBM in which 50-μm pitch microbumps and 8-μm pitch differential signaling channels were used to achieve 10 Gb/s per channel data rate [9]–[11]. Finally, 3-D integration can further improve interconnect density and reduce interconnect energy using through-silicon-vias (TSVs) for connectivity in the third dimension.

However, while silicon interposer and 3-D integrated systems are attractive due to the aforementioned benefits, cooling of these highly integrated systems is a challenge [12]. The 3-D integration presents a number of challenges to conventional forced-air cooling due to the large power density resulting from stacking multiple dice and the lack of direct access to the heat sink for dice within the stack (i.e., an air-cooled heat sink can only be attached to the topmost die in the stack). A promising solution to the cooling challenge is microfluidic cooling, which was first demonstrated in 1981 by Tuckerman *et al*. [13] in which the cooling of 790 W/cm^2 was demonstrated. More recently, Zhang *et al*. [14] reported a two-die stack with integrated micropin-fin heat sinks and demonstrated the cooling of $>$200 W/cm^2 at maximum junction temperature of 47 °C within each die.

Power delivery is another challenge for 3-D ICs. Power supply noise (PSN) results from current flowing across the parasitic resistance and inductance of the power delivery network [15], [16]. Multi-die stacks require high currents, and TSVs introduce higher resistance and inductance to the power delivery network. Thus, power delivery becomes more difficult for 3-D ICs [17], [18].

In this paper, novel electrical and fluidic microbumps are proposed to simultaneously enable high-bandwidth die-to-die signaling, embedded microfluidic cooling and power delivery for silicon interposer- and 3-D-based integrated systems. This paper is organized as follows: Section II describes 2.5-D and 3-D systems with embedded microfluidic cooling and the novel microbumps. In Section III, the design considerations of the fluidic microbumps are discussed. Section IV presents the fabrication process of the silicon dice and the interposer with the novel electrical and fluidic microbumps. Section V presents assembly and testing results. Section VI discusses PSN modeling and investigates PSN suppression methods. The conclusion is presented in Section VII.

II. Novel Electrical and Fluidic Microbumps

The proposed novel electrical and fluidic microbumps consist of an array of fine-pitch electrical microbumps with 25-μm

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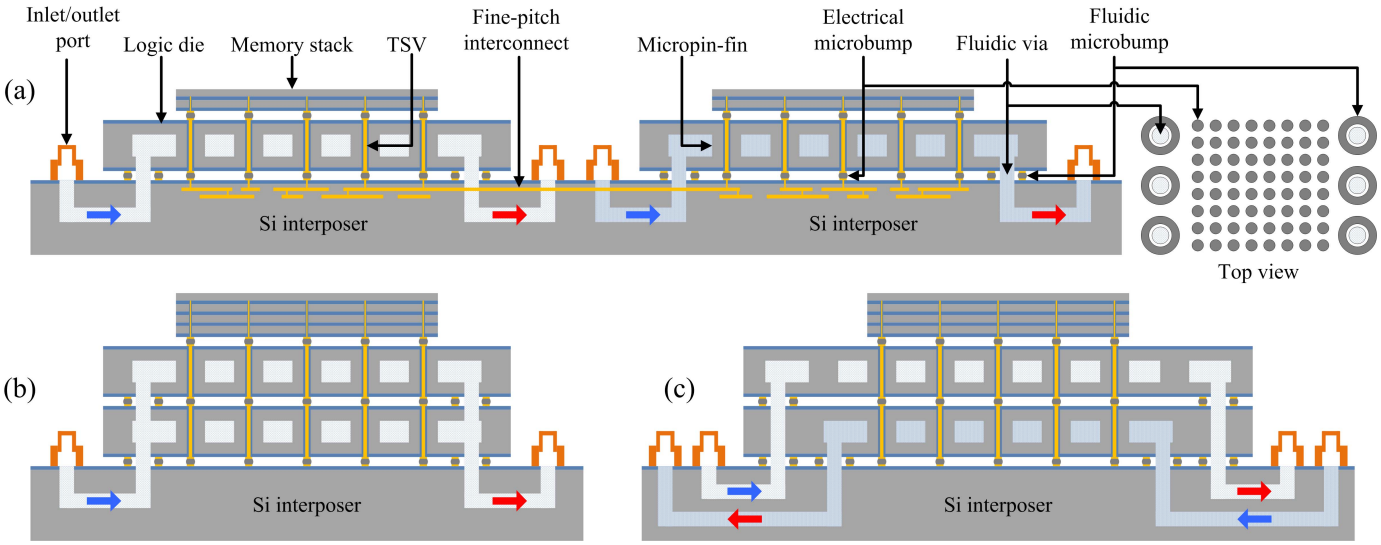

Fig. 1. Electrical and fluidic microbumps enabling high-bandwidth signaling and embedded microfluidic cooling for (a) 2.5-D interposer system of two logic dice and two memory stacks, (b) 3-D system of two logic dice and a memory stack, and (c) 3-D system with independent microfluidic cooling for each logic.

diameter and 50-μm pitch and two rows of annular-shaped fluidic microbumps. The electrical microbumps are used for signaling and power delivery, and the fluidic microbumps are used for microfluidic coolant delivery into/out of the die-level monolithic integrated microfluidic heat sink.

Fig. 1 shows three examples of silicon interposer- (2.5-D) and 3-D-based integrated systems using the novel microbumps. In Fig. 1(a), two logic dice, each with stacked memory, are assembled side by side on a silicon interposer. A top view of the microbumps is shown to the right in which a dense array of electrical microbumps are distributed over the die and a row of fluidic microbumps is placed on two opposite edges of the die. The coolant is delivered to the embedded micropin heat sink through the microchannels in the silicon interposer and fluidic vias and microbumps. After flowing across the micropin-fin heat sink and absorbing the heat, the coolant exits to the microchannels in the interposer through the fluidic vias and microbumps on the other edge of the die.

An SEM image of the embedded micropin-fin heat sink used in this paper is shown in Fig. 2. The micropin-fins are of 150-μm diameter, 225-μm pitch, and 200-μm height, and are directly etched on the back side of the logic die. The placement and dimensions of the staggered micropin-fins are based on previous optimization [19]. We have previously demonstrated this silicon micropin-fin heat sink dissipating 103.4 W/cm^2 at a junction temperature of 47.9 °C using a flow rate of 70 mL/min [20].

In addition to improved cooling capability, embedded microfluidic cooling eliminates bulky conventional air-cooled heat sink. Thus, the logic dice can be assembled in close proximity, and therefore, interconnect length can be reduced from several inches (board level wires) to a few millimeters (Si interposer level wires) [21], which significantly improves signaling bandwidth and energy dissipation.

Fig. 1(b) show a 3-D stack example consisting of two logic dice each with embedded micropin-fin heat sink and a memory stack above the logic dice. The two dice share one set of inlet/outlet ports. Thus, the flow direction in the two dice is the same and the flow rate cannot be adjusted independently for each die. Independent cooling is enabled by assigning dedicated inlet/outlet ports to each logic die, as shown in Fig. 1(c). With this configuration, the flow direction and rate can be independently adjusted for different cooling demands.

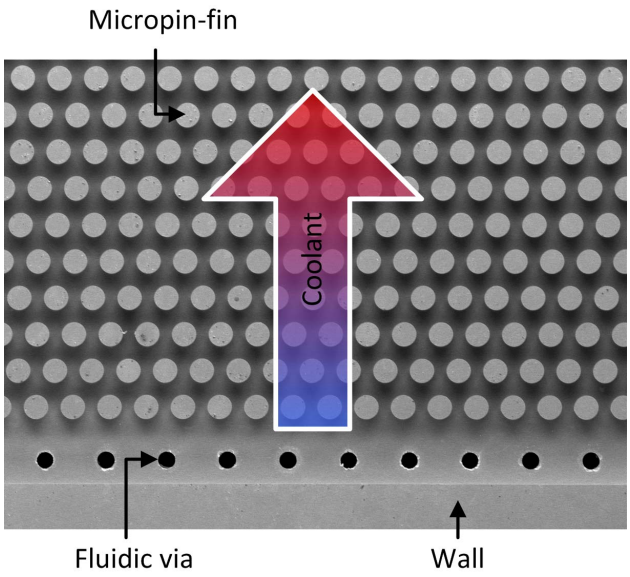

Fig. 2. Micropin-fins and fluidic vias etched on back side of a silicon die.

III. Fluidic Microbump Design

Annular-shaped fluidic microbumps are used to seal the fluidic vias. Therefore, the inner diameter of the microbump must be larger than that of the fluidic via. To determine the diameter of the fluidic vias, die area consumption and pressure drop within the vias must be considered. Larger fluidic vias

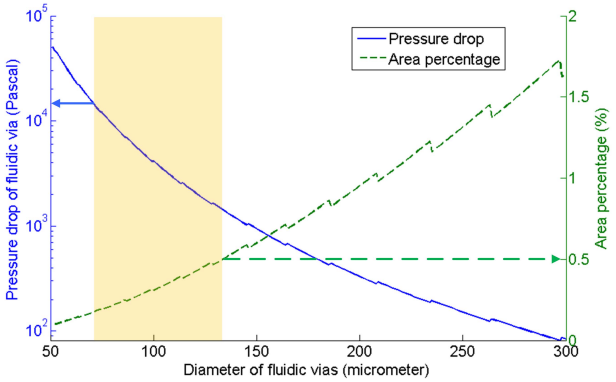

Fig. 3. Pressure drop within fluidic vias and percentage die area of fluidic vias as a function of fluidic via diameter.

reduce pressure drop but consume larger die area. Therefore, tradeoff analysis is needed to find an appropriate diameter.

The pressure drop within a fluidic via (in Pascal) is calculated using [22]

$$\Delta p = \frac{V^2 \cdot f \cdot L \cdot \rho}{2D} \tag{1}$$

where V is velocity in m/s, L is the length of the fluidic via, ρ is the coolant density in kg/m^3, D is the diameter of the fluidic via, and f is the friction factor. If the fluidic flow is laminar, the friction factor is calculated by

$$f = \frac{64}{Re} \tag{2}$$

where Re is Reynolds Number, which is calculated by

$$Re = \frac{1000 \cdot V \cdot D}{\nu} \tag{3}$$

where ν is kinematic viscosity in centistokes.

The percentage silicon die area dedicated to the fluidic vias can be simply calculated by

$$P = \frac{A_{\text{via}} \cdot N}{A_{\text{chip}}} = \frac{\pi \cdot (D/2)^2 \cdot N}{A_{\text{chip}}} \times 100\% \tag{4}$$

where A_{via} is the area of a fluidic via, N is the number of fluidic vias, and A_{chip} is the total die area.

Fig. 3 shows the pressure drop and the die area consumption as a function of fluidic via diameter for a fixed die edge length. Assuming that the length of the fluidic via is 200 μm, a flow rate of 70 mL/min, and the threshold for pressure drop within the fluidic vias and the total percentage die area consumption are 15 kPa and 0.5%, respectively, we find the feasible diameter range to be from ~70 to ~125 μm, as shown by the shaded region of Fig. 3. Based on this analysis, the fluidic via diameter chosen in this paper is 100 μm.

Spacing between the fluidic microbump inner-diameter and the fluidic via is required to avoid solder clogging and to compensate for flip-chip assembly alignment errors. Thus, the inner diameter of the fluidic microbumps was set to 150 μm leaving a 25 μm space between the edge of the fluidic via and the inner diameter of the fluidic microbump. The final dimensions of the electrical microbumps, the fluidic microbumps, and the fluidic vias are listed in Table I.

TABLE I
FINAL DIMENSIONS OF ELECTRICAL MICROBUMP, FLUIDIC MICROBUMP, AND FLUIDIC VIA

	Electrical microbump	Fluidic microbump	Fluidic via
Diameter	25 µm	150 µm (inner) 210 µm (outer)	100 µm
Pitch	50 µm	372.5 µm	372.5 µm

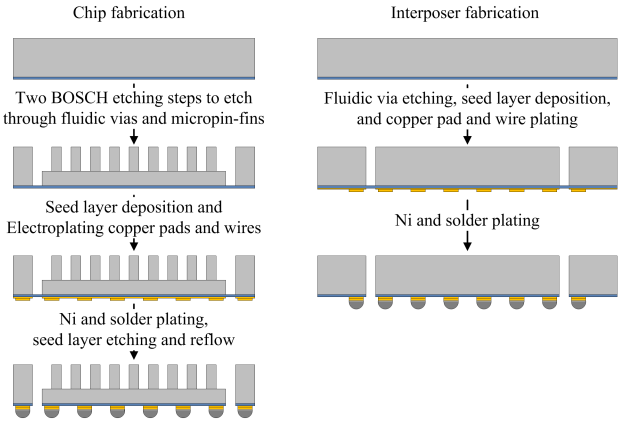

Fig. 4. Fabrication process for die and interposer.

IV. ELECTRICAL AND FLUIDIC INTERCONNECT FABRICATION

In this section, we discuss the fabrication of silicon dice and interposers with electrical and fluidic microbumps. The fabrication process for the silicon die is briefly described as follows: a layer of SiO_2 is deposited on the front side of a 4-in wafer as a dielectric layer. Following this process step, the micropin-fin heat sink and fluidic vias are etched on the back side of the wafer using two BOSCH etch steps. Next, a seed layer (Ti/Cu) is deposited on the front side for the electroplating of fine-pitch wires (8-μm width, 2-μm thick) and the copper pads for the electrical and fluidic microbumps. Next, Ni and solder are electroplated on the copper pads to form the electrical and fluidic microbumps. Following the electroplating step, the seed layer is stripped and the microbumps are reflowed. The silicon interposers used in this paper are fabricated using a similar process, as shown in Fig. 4; note no fluidic channels are made in the interposer in this paper to simplify the fabrication process.

Fig. 5 shows optical images of the fabricated die and interposer with high-density electrical microbump array ($150 \times 150 = 22500$ microbumps), two rows of fluidic microbumps (21 fluidic microbumps per row), and fine-pitch wires (8-μm width). Fig. 5(c) is a magnified image of the electrical and fluidic microbumps, the fluidic vias and the fine-pitch wires. Fig. 6 shows SEM images of the fabricated interconnect structures.

V. ASSEMBLY AND TESTING

The fabricated die was flip-chip bonded on a silicon interposer using a flip-chip bonder. After bonding, electrical and

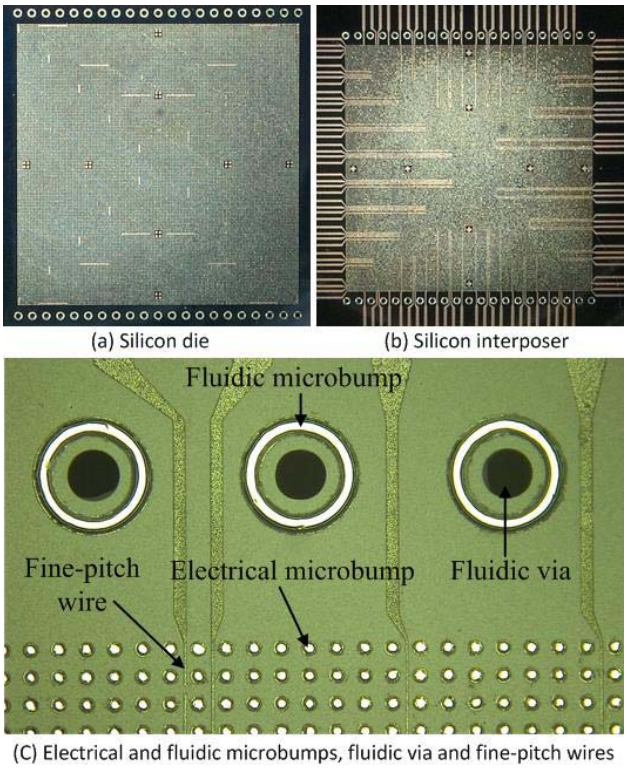

Fig. 5. (a) Top view of the die (top left). (b) Top view of the interposer (top right). (c) Close-up of electrical microbumps, fluidic microbumps, fluidic vias, and fine-pitch wires (bottom).

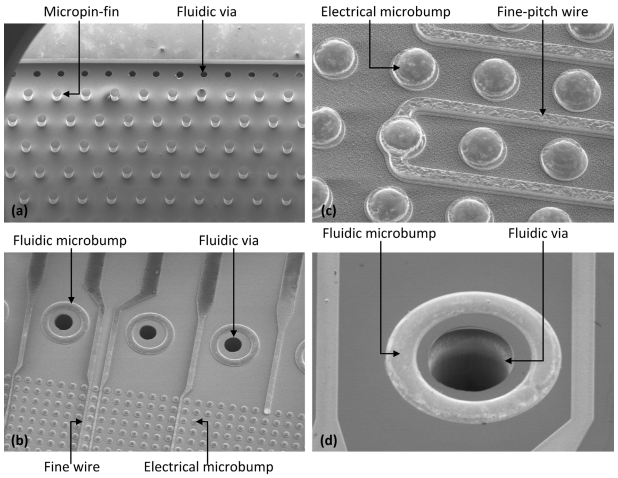

Fig. 6. SEM images of (a) micropin-fins and fluidic vias on the back side of the die, (b) electrical and fluidic microbumps, fluidic vias and fine-pitch wires, (c) close-up of electrical microbumps and fine-pitch wires, and (d) close-up of a fluidic microbump and a fluidic via.

fluidic tests were conducted to verify the electrical and fluidic interconnections.

A. Flip-Chip Bonding

Fig. 7 shows the flip-chip bonding process of the microfluidic cooled silicon die onto the silicon interposer. The details of the assembly process are listed in Table II.

Alignment accuracy is obviously critical to the success of the bonding. After bonding, X-ray images of the bonded sample were captured to check the alignment accuracy. Fig. 8

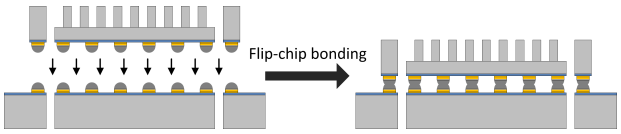

Fig. 7. Flip-chip bonding of the die and interposer with electrical and fluidic microbumps.

TABLE II
DIE AND BONDING PARAMETERS

Parameter	Value
Die size	~ 1 cm by 1cm
Number of fluidic microbumps	42 (21 each row)
Number of electrical microbumps	22,500 (150 by 150)
Temperature ramp rate	2 °C/s
Peak temperature	230 °C
Peak temperature duration	15 s
Bonding force	~7 N

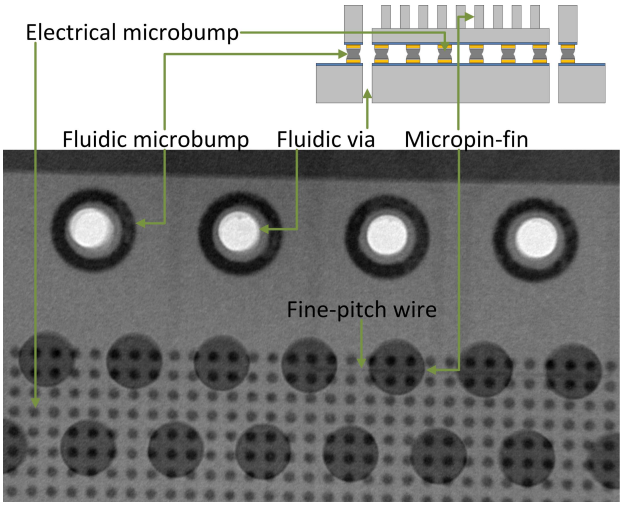

Fig. 8. X-ray image of the bonded die and interposer (top view).

shows the X-ray image of the bonded die and interposer, which illustrates good alignment.

B. Resistance Measurements

Following bonding, resistance of a single electrical microbump was measured using a four-point resistance measurement. Fine-pitch wires on the die and interposer are used to form the four-point measurement structure, as shown in Fig. 9. In Fig. 9(a), the light-colored wires are on the interposer, and the dark-colored wires are on the die. While the current is injected to the target microbump, the voltage drop across the microbump is measured to determine the resistance. Fig. 9(b) is the infrared (IR) image of the measurement structure.

Measurements were conducted on three bonded samples. Fig. 10 shows the measurement results. The average resistance of eight measured microbumps is 13.5 $\pm$1.82 mΩ. This result is consistent with the results reported in [9] demonstrating proper bonding.

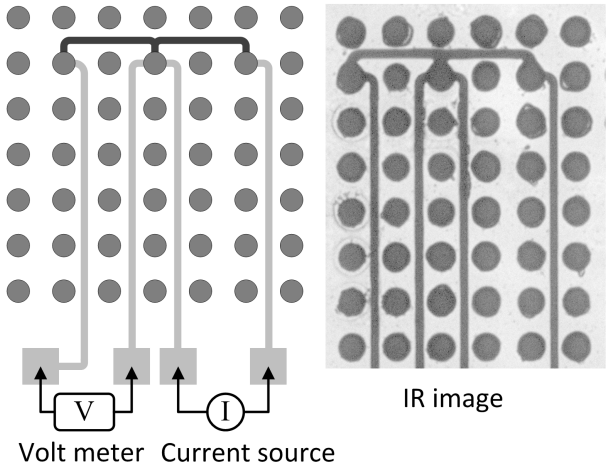

Fig. 9. (a) Four-point resistance measurement scheme for a single microbump. (b) IR image of the four-point measurement scheme.

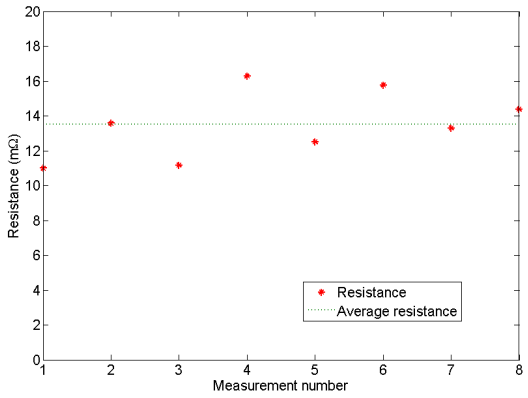

Fig. 10. Resistance of a single electrical microbump.

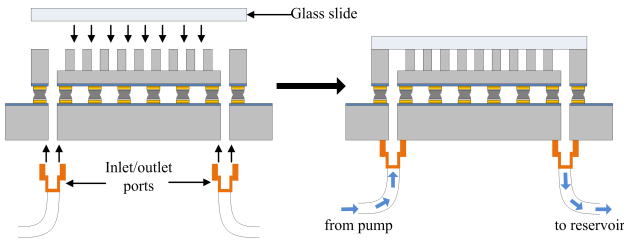

Fig. 11. Capping the micropin-fin heat sink and attaching inlet/outlet ports and tubes.

C. Fluidic Testing

Upon completion of the resistance measurement, a glass slide was used to seal the micropin-fin heat sink, and inlet/outlet ports and tubes were attached to the back side of the interposer to facilitate fluidic testing, as shown in Fig. 11.

During fluidic testing, DI water was pumped into the die, and the flow rate and pressure drop between the inlet and outlet ports (atmosphere pressure at outlet port) were recorded in real time. As expected, the pressure drop increases as flow rate increases, as shown in Fig. 12.

To test the preliminary reliability and sealing quality of the fluidic microbumps, DI water was pumped into the die continuously for 4 h at flow rates of 30 and 50 mL/min.

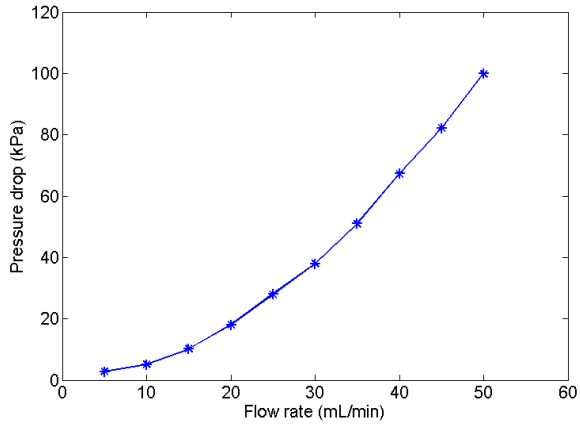

Fig. 12. Measured pressure drop as a function of flow rate.

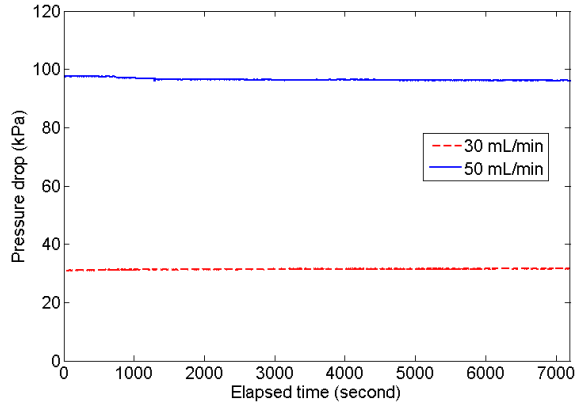

Fig. 13. Fluidic testing (continuous pumping DI water for 4 h, at flow rates of 30 and 50 ml/min).

No leakage was observed during testing. Fig. 13 shows the real-time pressure drop during the 4-h fluidic testing. The pressure drop is quite stable indicating no leakage occurred during the test, which was also consistent with visual inspection. These results indicate that the fluidic microbumps were well bonded.

VI. PSN Modeling

As previously mentioned, cooling and power delivery are two major challenges for future high-performance 3-D systems. Challenges in power delivery are discussed in this section.

According to 2011 ITRS, the supply voltage of future systems will decrease gradually, while the required current will slightly increase [23], as shown in Fig 14. The combination of decreasing supply voltage and increasing current complicates power delivery. 3-D stacking will further exacerbate the situation [24]. Moreover, the integration of an embedded microfluidic heat sink requires longer TSVs (larger resistive and inductive parasitics), which introduces new power delivery challenges, as shown in Fig. 15. Thus, it is important to understand the impact of an embedded microfluidic heat sink on power delivery and investigate effective ways to suppress PSN.

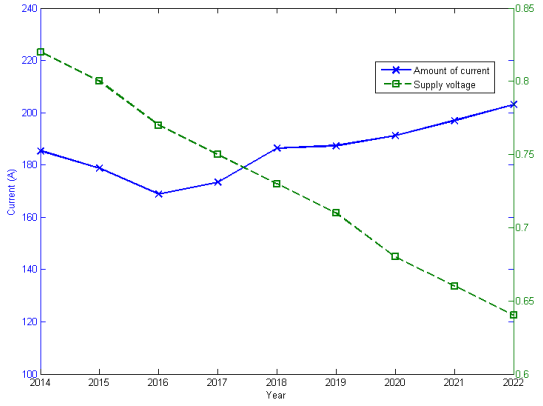

Fig. 14. Supply voltage and current drain projections for a single die (2011 ITRS).

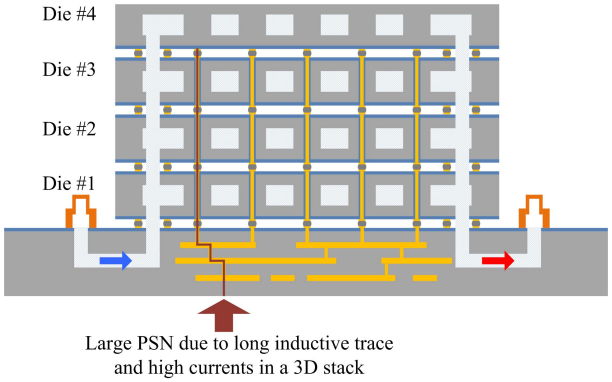

Fig. 15. Four microfluidic cooled dice 3-D integrated using TSVs.

A. Partial Differential Equations

Our model considers both IR drop and simultaneous switching noise and focuses on the first noise droop (midfrequency noise) [15], which results from the interaction of on-die decoupling capacitors and package inductance.

On-die global power distribution grids consist of power/ground pads and orthogonal interleaved power/ground interconnects on the top two metal layers, as shown in Fig. 16. Under the assumptions that the current density and the on-die decoupling capacitors are uniformly distributed, the girds can be divided into identical unit cells. Within each unit cell, two adjacent power/ground nodes and the area in-between can be modeled by the circuit model shown in Fig. 16, where R_s is the resistance of an interconnect segment connected to the node, Δ is the length of the segment, $J(s)$ is on-die current density in the frequency domain, and C_d is the on-die decap density. Based on this circuit model, partial differential equation (5) is derived to represent the voltage distribution within a unit cell (the derivation details in [17])

$$\nabla^2 V(x,y,s) = R_s J(s) + R_s V(x,y,s) 2sC_d + \Phi(x,y,s) \quad (5)$$

where $V(x,y,s)$ denotes the voltage level at location (xy) in a unit cell, $\Phi(x,y,s)$ is the source function of the partial differential equation (PDE) representing the voltage applied to

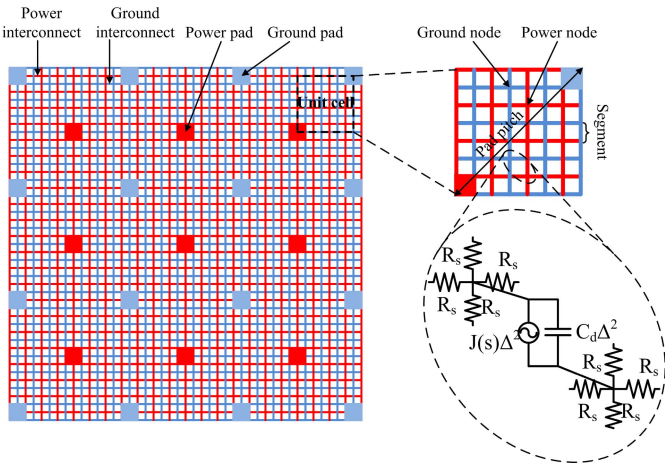

Fig. 16. On-die global power distribution grid is divided into unit cells, which are modeled by the simplified circuit.

the pad and can be expressed as

$$\Phi(x,y,s) = -R_s \frac{V(\alpha D_{\text{pad}}, 0, s)}{4(sL_p + R_p)} \delta(x)\delta(y) \quad (6)$$

where $V(\alpha D_{\text{pad}}, s)$ is the equivalent voltage at location $(\alpha D_{\text{pad}}, 0)$, assuming lower-left corner of the unit cell is the origin; α is a coefficient for pad shape [25], and D_{pad} is the side length of a quarter pad; L_p and R_p are the package inductance and resistance; $\delta(x)\delta(y)$ is the product of two delta functions, indicating the source is only applied to the origin.

Since it is assumed that current is uniformly distributed, no current flows across the four boundaries of the unit cell. Thus, the following boundary conditions are derived

$$\begin{aligned} \frac{\partial V(x,y,s)}{\partial x}|_{x=0} &= 0 \\ \frac{\partial V(x,y,s)}{\partial x}|_{x=a} &= 0 \\ \frac{\partial V(x,y,s)}{\partial y}|_{y=0} &= 0 \\ \frac{\partial V(x,y,s)}{\partial y}|_{y=a} &= 0 \end{aligned} \quad (7)$$

where a is the edge length of the unit cell.

Next, the model was expanded to 3-D grids by incorporating the TSVs. The following PDEs for 3-D grids were derived [17]:

$$\nabla^2 V_i(x,y,s) = R_{si} J_i(s) + R_{si} V_i(x,y,s) 2sC_{di} + \Phi_i(x,y,s) \quad (8)$$

where i indicates the i_{th} die in a stack.
The source function for die #1 is as follows:

$$\Phi_1(x,y,s) = -R_{s1}\left[\frac{V_1(\alpha D_{\text{pad}}, 0, s)}{4(sL_p + R_p)} + \frac{V_2(\alpha D_{\text{pad}}, 0, s) - V_1(\alpha D_{\text{pad}}, 0, s)}{4(sL_{\text{TSV}} + R_{\text{TSV}})}\right] \times \delta(x)\delta(y) \quad (9)$$

TABLE III
PARAMETERS OF THE 3-D DIE STACK

Parameters	Value
Number of stacked dice	4
Die thickness (TSV height)	50 μm
TSV diameter	10 μm
Die area	100 mm^2
On-die current density	1 A/mm^2
On-die decap percentage	10% of die area
Number of pad/TSV	2500
Pad/TSV pitch	202 μm
Pad shape parameter	0.2
Package inductance	0.5 nH
Wire segment length	28.3 μm
Wire width	2 μm
Wire thickness	1 μm

where L_{TSV} and R_{TSV} are the inductance and resistance of the TSV, respectively. The source function for die i is given by (10)

$$\Phi_i(x,y,s) = -R_{si}\left[\frac{V_i(\alpha D_{\mathrm{pad}},0,s)-V_{i-1}(\alpha D_{\mathrm{pad}},0,s)}{4(sL_{\mathrm{TSV}}+R_{\mathrm{TSV}})} + \frac{V_{i+1}(\alpha D_{\mathrm{pad}},0,s)-V_i(\alpha D_{\mathrm{pad}},0,s)}{4(sL_{\mathrm{TSV}}+R_{\mathrm{TSV}})}\right] \times\delta(x)\delta(y). \quad (10)$$

The boundary conditions for each die in the stack remain the same as in the 2-D case.

The set of frequency domain PDEs can be solved analytically [17], which enables a quick assessment of PSN for 3-D ICs.

B. PSN Analysis for 3-D Stacks and Implication on Power/Ground Pad Density

Based on the model described above, PSN of a 3-D stack consisting of four dice was simulated. Table III lists the parameters of the die stack. We assume homogeneous integrated dice in the stack and every die in the stack switching simultaneously for worst case PSN simulation.

Fig. 17 shows the PSN of each die in the stack. As expected, the PSN increases gradually from dies #1–#4, with die #4 having the maximum PSN (240.4 mV). Compared with the PSN of a single die (118.8 mV), PSN of the stack (die #4) increases by 102.4%. Next, the impact of die thickness on PSN was investigated, which is very relevant for dice with embedded microfluidic cooling. The die thickness increases from 50 to 250 μm due to the integration of the micropin-fin heat sink (all other parameters of the stack are unchanged). The PSN increases from dies #1–#4 with a maximum PSN of 377.3 mV, a 217.6% increase compared with the single die case, as shown in Fig. 17. Therefore, PSN suppression is critical for 3-D ICs. PSN of the two stacks are also simulated using HSPICE, as shown by the two dotted lines in Fig. 17. The difference between the compact model and HSPICE simulation is about 5%.

Increasing the number of power/ground pads is one of the effective ways of suppressing PSN. Fig. 18 shows the PSN

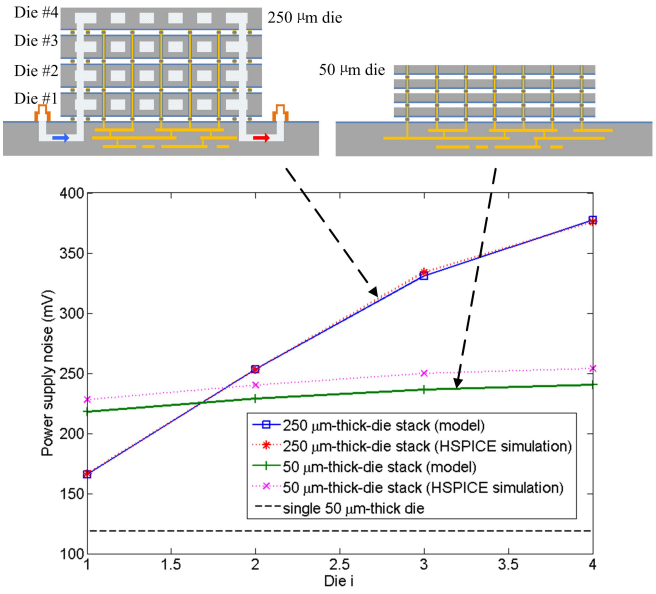

Fig. 17. PSN of two four-die stacks consisting of 50-μm thick dice and 250-μm thick dice, respectively.

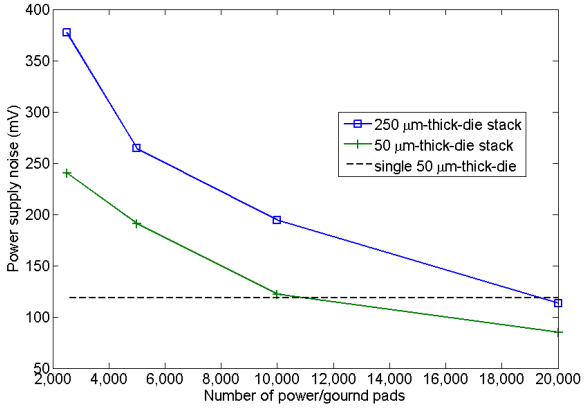

Fig. 18. PSN of two four-die stacks as a function of the number of power/ground pads.

of the two stacks (50-μm thick die and 250-μm thick die) as a function of the number of power/ground pads. The PSN is significantly reduced with increasing number of power/ground pads. For the 50-μm-thick-die stack, PSN of the stack drops to the single die level when the number of pads increases from approximately 2500 to 10 000. For the 250-μm-thick-die stack, approximately 20 000 power/ground pads are needed, as shown in Fig. 18.

Next, the impact of the number of dice in a stack was investigated. The PSN of a two-die stack (all other parameters unchanged from Table III) and a four-die stack are shown in Fig. 19. Obviously, PSN of the two-die stack (top most die) is less than that of the four-die stack. To achieve single die level PSN, the two-die stack requires approximately 5000 power/ground pads, while the four-die stack requires approximately 10 000 power/ground pads, as shown in Fig. 18.

Conventionally, PSN can be suppressed by increasing the amount of on-die decoupling capacitors, although this is costly. Fig. 20 compares the PSN of the four-die stack when the area

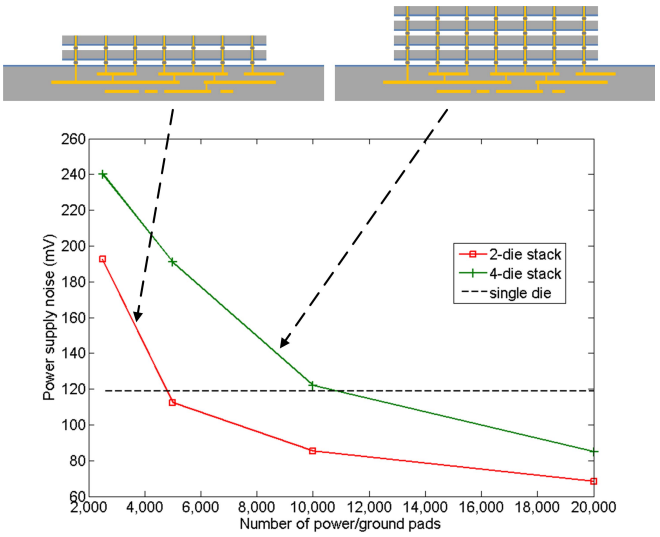

Fig. 19. PSN of a two- and a four-die stack as a function of the number of power/ground pads.

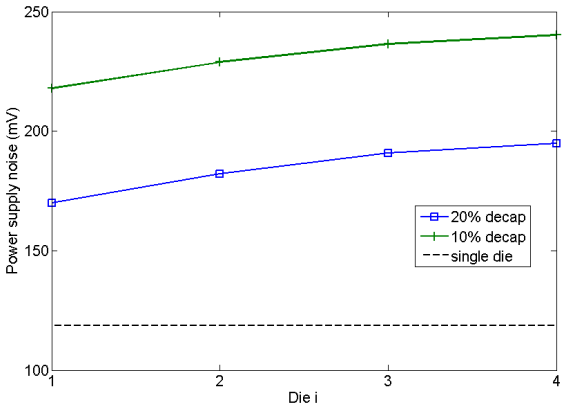

Fig. 20. PSN of two four-die stacks with 10% and 20% on-die decaps, respectively.

allocated to the decoupling capacitors in each die is increased from 10% to 20%. With 20% area allocation, the PSN is fairly well suppressed but still not close to the PSN of a single die. Potentially larger area for the decoupling capacitors might be needed, but of course this is cost prohibitive.

VII. Conclusion

Fine-pitch electrical microbumps (25-μm diameter and 50-μm pitch) and annular-shaped fluidic microbumps (150-μm inner diameter and 210-μm outer diameter) were designed and fabricated. Silicon dice with micropin-fin heat sinks and the novel electrical and fluidic microbumps were assembled on silicon interposers. Following assembly, electrical and fluidic testing verified electrical and fluidic bonding and demonstrated their feasibility. A compact physical model was used for PSN analysis. Increasing the number of power/ground pads is effective in suppressing the PSN of 3-D die stack, which necessitates fine-pitch microbumps from a power delivery point of view.

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